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Schwabe Williamson & Wyatt
PACWEST CENTER, SUITE 1900
1211 SW FIFTH AVENUE
PORTLAND, OR 97204

EXAMINER	
VU, TUAN A	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/544,894	DASU ET AL.	
	Examiner	Art Unit	
	TUAN A. VU	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 December 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *12,14-33 and 63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,26-33 and 63* is/are rejected.

7)☒ Claim(s) *14-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the Applicant's response filed 10/25/10.

As indicated in Applicant's response, claims 12-14 have been amended, and claims 1-11, 13, 34-62 canceled, and claim 63 added. Claims 12, 14-33, 63 are pending in the office action.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 63 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, claim 63 recites: determining a relative delay among possible paths through the common subgraph.

There insufficient description in the specifications for the mechanism of performing branch-and bound scheduling to "possible paths through the common subgraph" in conjunction with relative delay. Delays are computed with respect to apply path determination via PCP or DFGs, so that delays as tallied are computed and compared (Specifications: pg. 43), but not respect to a common sub-graph. The Appendix G describes sorting delay for worst delay and applying branch-and-bound scheduling whereas the scheduling algorithm applying to PCP and DFG extracted from a CDFG (Specs: pg. 43-45) has no mention of common subgraphs that include a longest-delay path or a relative delay, because nowhere this algorithm is tied to the

section describing "largest common subgraph" or "relative delay" depicted elsewhere in the Specifications. The Disclosure discusses LSCG, and common subexpressions, PCP and branch-and-bound heuristic all in differing contexts. No where is there description as to how a 'relative delay' is determined among possible paths through the common subgraph (emphasis added). As claim 63 does not correlate DFG, common subgraph with relative delay and/or longest delay path, one would recognize that the inventor is not in possession of 'relative delay' and a heuristic using relative delay or branch-and-bound that particularly addresses or implicates all possible 'paths through the common subgraph' as claimed. It is not clear how the invention would teach one skill in the art for make use of branch-and-bound (with relative delay paths determination approach) scheduling as disclosed to make it applicable to all possible paths through or relatively delayed with respect to LCSG (longest common subgraph) or 'common sub-expression', as this would require undue experimentation. Therefore, the requirement recited as 'for less than all possible paths through the common subgraph' (for branch-and-bound and relative delay) will not be given patentable merit; and will be treated as 'for all possible paths including at least a longest/relative delay.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12, 27-29, 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al, USPN: 20010016936 (herein Okada) in view of Hammes et al, USPN: 7, 155,708 (herein Hammes)

As per claim 12, Okada discloses a method comprising:

deriving control flow graphs for selected multiple program operations of a source code (Fig. 7-8; Fig. 21; para 0036, pg.3);

identifying code blocks of the control flow graphs; developing data flow graphs for two or more of the code blocks (para 0007 - pg 1; para 0036-0040, pg.3; para 0105-0110; Fig.26-27);

identifying a common subgraph shared by at least a pair of the code blocks (para 0166, 0174, pg 10; common node - para 0138, para 0145, para 0166) including identifying seed code blocks by identifying candidate seed code blocks among the basic blocks of the control flow graphs, and comparing candidate seed code blocks from control flow graphs of separate program operations (Fig. 28-30 – Note: comparing upper nodes based on a IF node comparison step prior to grouping the nodes into a common node **reads on** comparing candidate seed blocks of separated operations – see para 0131-0145,pg. 7-8);

scheduling the shared processes (para 0090, pg.5; Fig 7-8, Fig. 13; Fig. 30) represented by the common subgraph;

scheduling the shared processes for operation in each of the multiple program operations (see Fig. 30; para 0131-0145 pg.7-8 Note: use of selector to expand sub-CDFG logic scheduling to other sub-CDFG to achieve output resolution of operations of nodes within the synthesis context of a integrated circuit **reads on** scheduling i/o operations from blocks of control representing a shared block with respect to individual multiple operations construed via analyzed

nodes and validated input/output data from downstream subgraph nodes on the flow graph – S14, S15, Fig. 12; Fig. 40-43 and related text); and

scheduling of processing units to carry out the common subgraph (para 0106-110, pg. 6; Fig. 29; Fig. 37, 38, 41 - Note: scheduling based on selected path between branch operations involving unconditional/conditional edges and shared processes --Fig. 21-27; para 0166 – 0176 -- and forming a downstream common block – see: sel - Fig. 28, 34; Fig. 28-30 -- having internal node representing shared processes from upper nodes- see para 0135-0142).

Okada does not explicitly disclose code blocks being derived from the control graph or source code as basic blocks. The use of CDFG in terms of node being created as basic blocks is disclosed in **Hammes** (see Fig. 23-24; col. 7 lines 54-62); and based on the similarity by which input and output from nodes in Okada and Hammes are analyzed its most simplified form and submitted to a scheduler (see Okada: para 0090-0096; Hammes: Fig. 23-24) it would have been obvious for one of ordinary skill in the art to implement the pre-arranging of control flow graph in Okada so that these become basic block associated with data in/out operations as the context that they are sequentially analyzed along with scheduling of nodes with respect to their associated data dependency in its serial basic form as shown in Hammes (col. 21 line 63 to col. 22 line 21) because validation by a scheduler in regard to dependency of data associated to a basic block node without bifurcated I/O edges would be highly facilitated.

As per claim 27, Okada discloses ASIC as conventionally a field of design where high-level synthesis would be used to reduce size (para 0004, para 0041), hence it would have been obvious for one of ordinary skill in the art to implement Okada in providing the common operations of the common subgraph so that this providing would be for an application specific

integrated circuit, because of the well-known applicability of high-level synthesis in reducing size of the surface to implement the circuit.

As per claim 28, Okada discloses:

identifying at least one other common subgraph shared by the at least a pair of the basic blocks (refer to claim 1); but does not explicitly disclose:

(i) scheduling other shared processes represented by the other common subgraph; scheduling the other shared processes for operation in individual ones of the multiple program operations; and

(ii) laying out another arrangement of other circuit elements for implementation of the integrated circuit in hardware, including:

(iii) grouping the other circuit elements into other first level clusters; and

(iv) placing the other first level clusters by grouping the other first level clusters together to form other second level clusters and placing the other second level clusters.

Okada discloses ASIC as conventionally a field of design where high-level synthesis would be used to reduce size (para 0004, para 0041). In view of the intent to systematically address all level of the CFG and the modified aspect of the modified subgraphs via scheduling and grouping, the above steps (i) to (ii) along with (iii) and (iv) would have been obvious, because any other shared process not addressed in the synthesis and hardware placing via the process included in the layered clustering or grouping as set forth in claim 12 would fail to achieve the size reducing contemplated in Okada's high-level synthesis and hardware allocation and chip building as purported.

As per claim 29, Okada does not explicitly disclose identifying a largest common subgraph shared by the at least a pair of the basic blocks; however, this limitation has been addressed in claim 1.

As per claim 32, refer to claim 27.

As per claim 33, refer to computer-readable medium (Okada: claim 8 - pg. 8) to perform the method of claim 12.

6. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al, USPN: 20010016936 (herein Okada) in view of Hammes et al, USPN: 7, 155,708 (herein Hammes) further in view Cheng et al, "High-Level synthesis: Current Status and Future Prospects", June 1993 pp. 351-400 (herein Cheng)

As per claim 26, Okada does not explicitly disclose wherein said scheduling the shared processes represented by the common subgraph includes comprises ASAP scheduling the common subgraph. Cheng discloses use of branch-and-bound to complement heuristics with identification of critical path, mobility of resources, all of which scheduling aspects considered integral to a preliminary algorithm known a constructive or iterative algorithm (sec 3.11.2 pg. 361 to 363) which also includes analyzing CFG and DFG with ASAP approaches for finding boundaries of resources. It would have been obvious for one of ordinary skill in the art to implement the resources finding and execution time related thereto in Okada (see claim 12) so that a ASAP approach would be applied because this would effectuate a non-exhaustive collection of data needed for the latter stage of scheduling to implement branch-and-bound heuristics for the reasons set forth in claim 12, in view of the proposed approaches laid out in Cheng.

7. Claims 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al, USPN: 20010016936 (herein Okada) and Hammes et al, USPN: 7, 155,708 (herein Hammes), further in view of APA(Admitted Prior Art: Specifications pg. 8-10) and Bertolet et al, USPN: 5,671,432 (herein Bertolet)

As per claim 30-31, Okada does not explicitly disclose (scheduling shared processes represented by common subgraph) with providing switching of differing delays among processes of the common subgraph to effect subgraphs operating each individual ones of the selected multiple program operations, including providing multiplexers operative to apply alternative delays between processes of the common subgraph.

Okada discloses grouping of CDF elements (e.g. para 0135-0153) using analytical synthesis of requirement between nodes or graph elements to move or replace them in an effort to reduce scale (para 0098, 0104, 0161, 0163) of area chosen to implement the corresponding hardware circuit elements. Analogous to the designing of integrated circuit of Okada, APA discloses chip design with partitioning of blocks into sub-blocks of the hardware elements in area of surface substrate (surface planning, recursively into smaller blocks – APA, pg. 9), with routing of interconnections and portioning, placement and routing (APA, Specs pg. 8) using iterative placement until size of chip is reduced (APA, pg. 9-10). Similar to designing hardware and using of FPGA (see APA: pg. 3, 9) in support for applications to configure ASIC architecture as in Okada, **Bertolet** discloses conductor and switches among the integrated gates so to enable conduction and propagation with selective control passing between bus support of the interconnected programmable elements (col. 5 lines 4-23).

Okada discloses circuit implementation with multiple inputs and a selector (e.g. Fig. 9, 16, 28, 34) which is reminiscent of a MUX gate, a HW concept along with that of switches which were also mentioned in Cheng (see Cheng: MUXes – middle pg. 379; Muxes, Switches - Table 1 - pg. 354) whereas the concept of using a switch to transfer control among alternated data flow or bus related to other gates is disclosed in Bertolet. Thus, it would have been obvious for one skill in the art at the time the invention was made to implememt a switching or selector functionality among different subgraphs such as switches or multiplexers operative to apply alternative delays between processes of the common subgraph as taught in Okada so that conductors and switches among blocks, subblocks and circuit elements – as taught in Bertolet - were used to effect selection or variation of paths among the interconnected elements as taught, as this would enhance the iterative placement and reconfiguration endeavor adapted to effectuate the best optimized path transmission (i.e. via selective switching of transfer) leading to minimized consumption of power so well contemplated in the field of FPGA design and integrated circuit building.

8. Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al, USPN: 20010016936 (herein Okada) in view of Hammes et al, USPN: 7, 155,708 (herein Hammes) in view of Cheng et al, "High-Level synthesis: Current Status and Future Prospects", June 1993 pp. 351-400 (herein Cheng); further in view of Brisk et al, "Instruction Generation and Regularity Extraction for Reconfigurable Processors", CASES 2002, Oct 2002 (herein Brisk); and Janssen et al, "A Specification Invariant Technique for Regularity Improvement between Flow-Graph Clusters (herein Janssen)

As per claim 63, Okada discloses wherein said scheduling of processing units to carry out the common subgraph (see claim 12); laying out an arrangement of circuit elements for implementation of the integrated circuit in hardware (laying out an arrangement of circuit elements for implementation of the integrated circuit in hardware (Fig 12)

However, Okada does not explicitly disclose clustering the shared processes into a macroblock having nodes representing the shared processes and at least a plurality of unconditional, conditional, and reconfiguration edges running between nodes

Okada discloses grouping (para 0135-0142) and scheduling based on selected path between branch operations involving unconditional/conditional edges and shared processes (Fig. 21-27; para 0166 - 0176) and forming a macro version as common block (e.g. sel - Fig. 28, 34) having internal node representing shared processes from upper nodes. The concept of shared process as subgraph or similar to a macroblock is disclosed in the regularity detection by Brisk with use of templates to support heuristics for parallel and sequential clustering (see Brisk: sec 3-4 pg. 2-5) and the resource sharing cluster by Janssen (Janssen: sec 2-4 pg. 139-142) in which merging would capitalize the heuristics or combine elementary transformations (see Brisk: sec 4.1 pg. 5; see Janssen: composite transformation pg. 142). It would have been obvious for one of ordinary skill in the art to implement the grouping and scheduling of unconditional/condition edges between branch in Okada so that substitution of shared processes would be as a macro-block subgraph including nodes representing operations related to those unconditional/condition edges, such that reconfiguring would be based on those edges as taught in the template-based heuristics of Brisk or in view of shared-resource transformation in Janssen, because clustering of individual node operations representing intermediate edges (prior to branching) would enable

resolution of data requirement while simplifying the layout of the complex flow graph elements; e.g. by replacing shared subexpression or common resource operations with a common macroblock; which facilitate allocation needed to implement the hardware physical layout (see Okada: Fig 12; para 0132-0133) pertinent to the ASIC development.

Nor does Okada explicitly disclose: determining a relative delay among possible paths through the common subgraph (refer to USC 112 Rejection); performing branch and bound scheduling for the longest-delay-time path; merging all schedules.

The identification of delay among edges or path length was a known concern when deriving source code into CDFG and basic blocks from its DAG in the endeavor for scheduling and implementing hardware therefrom, as this is shown in Okada (operating time – para 0029-0030) and Hammes (Fig. 27), whereas applying of branch-and-bound heuristic is disclosed in Cheng as a technique used so to improve upon scheduling or sorting based on resources availability or register limitation derived along critical path or mobility (Cheng: pg. 363) or upon any phase related to resource allocation or look ahead heuristics (pg. 374-376), including variable binding or data transfer (pg. 386) and where delay-cost or area-cost can be complemented with branch-and-bound technology in the netlist synthesis approach (pg. 391, bottom); where scheduling procedures in terms of binding or data path allocation concerns with longest delay path that would not exceed a threshold (pg. 383) which is analogous to the concept of not exceeding a time in Okada (see Okada: para 0099, 0151). Based on the endeavor to localize delay and resources usage between node on the graph (e.g. DFG in Hammes) and in view of minimizing hardware placement area (surface size) in Okada's high-synthesis and path analysis with time threshold concerns according to Cheng proposals and Okada's path analysis, it

would have been obvious for one of ordinary skill in the art to implement the scheduling in Okada so that delay is determined in conjunction of resources/register analysis respective to processes on the control graph (e.g. via basic block requirement between edges as in Hammes delay determination) with delay in terms of relative or longest delay paths, so that all possible paths analyzed in heuristics about resource availability or input/output requirement, register limitation, variable binding, delay cost determination as set forth above would be enhanced by a branch-and-bound scheduling as taught in Cheng. One would be motivated to do so because this would fine tune the results afforded from the search regarding cost caused by possible path delay (relative or longest) set forth in Okada or Hammes, in view of the branch-and-bound approach positive benefits identified in Cheng from above.

Nor does Okada disclose layout or merging of schedules including:

grouping the circuit elements into first level clusters; and placing the first level clusters by grouping the first level clusters together to form second level clusters and placing the second level clusters.

Nor does Okada explicitly disclose merging all schedules including: grouping the circuit elements into first level clusters; and placing the first level clusters by grouping the first level clusters together to form second level clusters and placing the second level clusters.

The grouping of nodes in terms of cluster is disclosed in Brisk where combining results from either parallel/sequential clustering whereas transformation from elementary to composite is effectuated in Janssen's technique to identify shared resources (see above). Based on the well-known concept in ASIC design with reconfigurable elements where placement of HW element is based on scheduling prior to allocation and layout, the grouping of first level cluster and second

level clusters in view of the high-level synthesis would be deemed obvious. It would have been obvious for one of ordinary skill in the art to implement the grouping and analysis of data dependency related to shared processes as in Okada in view of both Brisk and Janssen, so that circuit elements are grouped based on such synthesis and clustering approach, including placing the first level clusters by grouping the first level clusters together to form second level clusters and placing the second level clusters, because this placement would be the ultimate phase for which detection of shared processes, resources or subgraphs has been extensively employed – as per Brisk, Janssen and even Okada -- in any stage prior to the allocation phase.

Allowable Subject Matter

9. Claims 14-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten (i.e. as indicated in the whole combination from below) in independent form including all of the limitations of the base claim and any intervening claims.

The subject matter deemed allowable contains:

(a) identifying seed basic blocks by identifying candidate seed basic blocks among the identified basic blocks of the of control flow graphs, and comparing candidate seed basic blocks from control flow graphs of separate program operations.

identifying ones of the basic blocks that lie inside a loop, including ones of: a single nested level loop with only one basic block; a single nested level loop with more than one basic block; and a multi-level nested loop, a single nested level loop with more than one basic block; and a multi-level nested loop

(b) identifying basic blocks of control flow graphs of separate program operations under like control; determining a count of individual operation types in a basic block, including

examining edges in a data flow graph of candidate seed basic blocks of control flow graphs from the separate programming operations; classifying edges based on source and destination node operation type;

(c) wherein said examining edges includes eliminating edges of one data flow graph having a source-operation-to-destination-operation not found in another data flow graph having edges under examination; implementing the eliminated edges in a circuit other than in an application specific integrated; implementing the eliminated edges with in one or more look up tables.

Interview Summary

10. A telephone contact was initiated by the Examiner in order to seek additional insights from the representative, Mr. Richard Legett, on 12/14/10, regarding how the limitations of claims 13-25 correlate to the crux of the independent claim subject matter, in order to derive a allowable independent scenario with a more focused embodiment (as opposed to listing of heterogeneous algorithmic approaches); but no agreeable terms was reached.

Response to Arguments

11. Applicant's arguments filed 10/25/10 have been fully considered but they are not persuasive. Following are the Examiner's observation in regard thereto.

(A) Applicants have submitted that claim 12 has been added the matter of claim 13 which was indicated as "allowable" by the Office; hence would be allowable (Appl. Rmrks pg. 8). The amended claim 12 has necessitated a new ground of rejection, and the argument would be deemed non-commensurate with this ground of rejection.

(B) Applicants have submitted that claim 63 is in condition for dependency upon allowable claim 12 (Appl. Rmrks pg. 8). This would be referred to section A.

The claims as submitted will stand rejected as set forth in the Office Action.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (571) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571)272-3759.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence - please consult Examiner before

using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Tuan A Vu/

Primary Examiner, Art Unit 2193

December 26, 2010